What is claimed is:

1. A program voltage generation circuit in a flash memory, for achieving stable programming of flash memory cells, the program voltage generation circuit comprising:

a constant current source which provides a sink current;

a program wordline voltage generation unit which generates a program wordline voltage applied to the gate of a flash memory cell, in response to the sink current and the result of a comparison between a reference voltage and a bitline voltage;

a bitline voltage generation unit which generates the bitline voltage according to a program current flowing to the first flash memory cell; and

a bitline current control voltage generation unit which generates a bitline current control voltage in response to the program current that flows to a second flash memory cell in response to the program wordline voltage.

2. The program voltage generation circuit of claim 1, wherein the program wordline voltage generation unit comprises:

a first PMOS transistor which has a source coupled to a power supply voltage and a gate and a drain that are coupled to each other;

a first NMOS transistor which has a source coupled to a ground voltage and a gate and a drain that are coupled to each other, and is coupled to the drain of the PMOS transistor;

a second NMOS transistor which has a source coupled to the ground voltage, a gate coupled to the gate of the first NMOS transistor to form a current mirror, and a drain coupled to the program wordline voltage;

a second PMOS transistor which is connected between the power supply voltage and the drain of the second NMOS transistor and has a gate coupled to an output of a voltage comparator; and

the voltage comparator which compares the bitline voltage with the reference voltage and provides the output corresponding to the result of the comparison to the gate of the second PMOS transistor.

3. The program voltage generation circuit of claim 1, wherein the bitline voltage generation unit comprises:

the first flash memory cell which has a source coupled to a source voltage and a gate coupled to the program wordline voltage; and

a resistor which is coupled between the drain of the first flash memory cell and the ground voltage and generates the bitline voltage.

4. The program voltage generation circuit of claim 1, wherein the bitline current control voltage generation unit comprises:

a second flash memory cell which has a source coupled to a source voltage and a gate coupled to the program wordline voltage; and

an NMOS transistor which has a source coupled to a ground voltage and a gate and a drain that are coupled to the drain of the second flash memory cell and generate the bitline current control voltage.

5. The program voltage generation circuit of claim 4, wherein the flash memory device comprises:

a flash memory cell in a flash memory cell core array to be programmed, which has a gate coupled to the program wordline voltage, a source coupled to the source voltage, and a drain coupled to the bitline voltage; and

an NMOS transistor gated to the bitline current control voltage between the drain of the flash memory cell and the ground voltage.

6. A program voltage generation circuit in a flash memory, for achieving stable programming of flash memory cells, the program voltage generation circuit comprising:

a constant current source which includes a first PMOS transistor and first and second NMOS transistors, wherein the first PMOS transistor has a source coupled to a power supply voltage and a gate and a drain that are coupled to each other, the first NMOS transistor has a source coupled to a ground voltage and a gate and a drain that are coupled to each other, and is coupled to the drain of the first PMOS transistor, and

the second NMOS transistor has a source coupled to the ground voltage, a gate coupled to the gate of the first NMOS transistor to form a current mirror, and a drain coupled to the program wordline voltage;

a second PMOS transistor which is connected between the power supply voltage and the drain of the second NMOS transistor and has a gate coupled to an output of a voltage comparator;

the voltage comparator which compares the bitline voltage with a reference voltage and provides the output corresponding to the result of the comparison to the gate of the second PMOS transistor;

a first flash memory cell which has a source coupled to a source voltage and a gate coupled to the program wordline voltage;

a resistor which is coupled between the drain of the first flash memory cell and the ground voltage and generates the bitline voltage according to a program current flowing to the first flash memory cell;

a second flash memory cell which has a source coupled to a source voltage and a gate coupled to the program wordline voltage; and

an NMOS transistor which has a source coupled to a ground voltage and a gate and a drain that are coupled to the drain of the second flash memory cell and generate a bitline current control voltage according to a program current flowing to the second flash memory cell.

7. The program voltage generation circuit of claim 6, wherein the flash memory device comprises:

a flash memory cell in a flash memory cell core array to be programmed, which has a gate coupled to the program wordline voltage, a source coupled to the source voltage, and a drain coupled to the bitline voltage; and

an NMOS transistor gated to the bitline current control voltage between the drain of the flash memory cell and the ground voltage.

8. A method of programming a flash memory cell, the method comprising:

supplying a sink current from a constant current source;

generating a program wordline voltage applied to the gate of a flash memory cell, in response to the sink current and the result of a comparison between a reference voltage and a bitline voltage;

generating the bitline voltage to be applied to the drain of the first flash memory cell, according to a program current flowing to the first flash memory cell;

generating a bitline current control voltage in response to the program current by applying the program wordline voltage to the gate of a second flash memory cell; and

programming the flash memory cell by flowing the program current to the flash memory cell by applying the program wordline voltage to the gate of the flash memory cell, the bitline voltage to the drain of the flash memory cell, and the bitline current control voltage to the gate of an NMOS transistor coupled between the flash memory cell and a ground voltage.